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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/711,838	11/13/2000	Wei Pin Chen	JCLA5123	7804
7590	03/25/2004		EXAMINER	
J C Patents Inc 4 VENTURE Suite 250 Irvine, CA 92618			MARCELO, MELVIN C	
		ART UNIT	PAPER NUMBER	
		2663	S	

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/711,838	CHEN ET AL.
	Examiner Melvin Marcelo	Art Unit 2663

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 13 November 2000.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-16 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-16 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 13 November 2000 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 7, 10-12 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by DeJager et al. (US 6473424 B1).

With respect to the claims, references to DeJager appear in parenthesis.

1. A relay control circuit for use in a Switch device having a number of ports (DeJager, Figures 2 and 4, and column 1, lines 10-27)), for the purpose of performing load-balancing in the Switch device based on a port group configuration (Column 1, lines 38-44); the Switch device including an address-extraction circuit for extracting an address information from a received frame (Destination and source addresses in Figure 2 and column 5, lines 7-13) and a memory unit for storing a routing table (StreamState Table in Figure 2 and column 5, lines 42-45); the relay control circuit comprising: a transformation circuit for transforming the address information into an index address (Stream identification, column 5, lines 14-15 and 42-45); a storage unit for storing the port group configuration which is adjustable (Figure 4, registers 408, 410, 412, 414, 418 and 420, used for storing current port group configuration, column 9, lines 27-55); and a comparison circuit for forwarding the received frame according to the index address and the port group configuration (Column 7, lines 6-43); wherein the port group configuration contains arbitrary number of ports (Column 1, lines 38-44), and is adjusted according to a frame throughput of the ports (Column 9, lines 27-55).

2. The circuit of claim 1, wherein the port group configuration includes a plurality of certain ports assigned to a port group

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(Column 1, lines 38-44) and a load-balancing relationship between the index address and the certain ports (Load-balancing is based on the index address-stream ID, column 7, line 59 to column 8, line 31), adjusting the load-balancing relationship between the index address and the certain ports belonging to the port group if the frame throughput of any of the certain ports is over-loading (Column 8, line 32-50, wherein the volume of different streams and stream activity can be that they are over-loading the queue belonging to a certain port).

7. A relay control method for forwarding a frame with an address information in a Switch device, the Switch device having a number of ports (Column 3, lines 16-18) and a routing table based on a port group configuration (Column 3, lines 31-32, stream state table); the method comprising the steps of: transforming the address information into an index address (Column 3, line 24-31, hashing of the address); forwarding the frame according to the index address, the routing table, and the port group configuration (Column 3, lines 16-38); and adjusting the port group configuration if an over-loading is occurred in the ports (Column 8, line 32-50, wherein the volume of different streams and stream activity can be that they are over-loading the queue belonging to a certain port).

10. The method of claim 7, wherein the address information includes the source and destination of the frame (Column 5, lines 10-18).

11. The method of claim 7, wherein the port group configuration includes a plurality of certain ports assigned to a port group (Column 1, lines 38-44) and a load-balancing relationship between the index address and the certain ports (Load-balancing is based on the index address-stream ID, column 7, line 59 to column 8, line 31), adjusting the load-balancing relationship between the index address and the certain ports belonging to the port group if the over-loading is occurred in the ports (Column 8, line 32-50, wherein the volume of different streams and stream activity can be that they are over-loading the queue belonging to a certain port).

12. A Switch device for forwarding a frame comprising: an address-extraction circuit for extracting an address information from the frame (Column 5, lines 7-18); a memory unit for storing a routing table (Figure 2, StreamState Table); and a relay control circuit, the relay control circuit transforming the address information into an index address (Column 5, lines 42-45), storing a port group configuration (Column 9, lines 34-55), and forwarding the frame according to the index address, the

*routing table, and the port group configuration (Column 9, lines 17-55); wherein the port group configuration is adjusted based on the throughput in the Switch device (Column 9, lines 46, dynamic load balancing).*

15. *The Switch device of claim 12 wherein the relay control circuit further includes:*

*a storage unit for storing the port group configuration (Figure 4, Registers 408, 410, 412, 414, 418, 420).*

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 5, 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeJager et al.

DeJager does not teach that the storage register is an EEPROM or that a DIP switch is used to set the port group configuration. However, both the EEPROM and DIP switch are well known electrical devices. The EEPROM is a commercially available storage device and the DIP switch is a commercially available input device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an EEPROM for the registers storing the data in DeJager since a skilled artisan would have been motivated to use readily available devices. With respect to the DIP switch, a skilled artisan would have been motivated to provide manual control over the settings in the register for such purposes as testing or personal preferences over which ports to use. Therefore, it would have been obvious to provide

a DIP switch in DeJager for the reason that a user may want to test the settings or have personal preferences in the ports. With respect to the claims, references to the prior art appear in parenthesis.

5. *The circuit of claim 1, wherein the storage unit is EEPROM (Commercially available).*
6. *The circuit of claim 1, wherein the port group configuration are set through a DIP switch (Commercially available for use in manually setting input data).*
16. *The Switch device of claim 15 wherein the storage unit is EEPROM.*

5. Claims 3, 4, 8, 9, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeJager et al. in view of Liu et al. (US 6018526).

DeJager does not teach the transformation (hash) circuit is a CRC circuit that is an 8 bit modulo. However, DeJager explicitly suggests using other hashing techniques (column 5 lines 28-30). Liu teaches a hashing technique that is a CRC circuit that results in an 8 bit modulo index address (column 9, lines 45-64, most significant 8 bits of the CRC). Therefore, it would have been obvious to use Liu's hashing technique in DeJager since a skilled artisan would have been motivated by DeJager's suggestion to use other hashing techniques.

3. *The circuit of claim 1, wherein the transformation circuit is a cyclic redundancy check (CRC) circuit and the index address is a CRC modulo (Liu, column 9, lines 45-64).*
4. *The circuit of claim 3, wherein the CRC modulo is 8 bit in length (Liu, column 9, lines 45-64).*
8. *The method of claim 7, wherein the step of transforming the address information into the index address is performed by a CRC operation and the index address is a CRC modulo.*
9. *The method of claim 8, wherein the CRC modulo is 8 bit in length.*

13. The Switch device of claim 12 wherein the relay control circuit includes a CRC circuit for transforming the address information into the index address, and the index address is a CRC modulo.

14. The Switch device of claim 13 wherein the CRC modulo is 8 bit in length.

**Conclusion**

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wong et al. (US 6614758) teach another load balancing port group switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Marcelo whose telephone number is 703-305-4373. The examiner can normally be reached on Monday-Friday, 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 703-308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Melvin Marcelo  
Primary Examiner  
Art Unit 2663

March 20, 2004